What is claimed is:

1. A field effect transistor comprising, in combination:

a) a substrate having a substantially-planar upper substrate surface;

b) an elongated channel of semiconductor material, said elongated channel being inclined with respect to said upper substrate surface;

c) said channel including a top and a bottom with the bottom of the channel contacting said upper substrate surface;

d) said substrate being substantially conductive in the region contacting said bottom of said elongated channel;

e) said channel including a heavily doped region adjacent the top thereof; and

f) a gate comprising a planar layer of conductive material arranged substantially parallel to said upper substrate surface.

2. A field effect transistor as defined in Claim 1 further including a gate insulator layer substantially surrounding the length of said elongated channel.

3. A field effect transistor as defined in Claim 1 further including a first substantially-planar insulating layer between said gate and said upper substrate surface.

4. A field effect transistor as defined in Claim 3 further including a second substantially-planar insulating layer overlying said gate.

5. A field effect transistor as defined in Claim 2 further including a layer of conductive material in contact with said gate and substantially surrounding the length of said elongated channel.

6. A field effect transistor as defined in Claim 1 wherein said substrate is of semiconductor material.

7. A field effect transistor as defined in Claim 6 wherein said semiconductor material is globally moderately-doped and includes a locally highly-doped region adjacent the bottom of said elongated channel.

8. A field effect transistor as defined in Claim 6 wherein said semiconductor material is globally heavily-doped.

9. A field effect transistor as defined in Claim 1 wherein said elongated channel comprises silicon.

10. A field effect transistor as defined in Claim 1 further characterized in that:

a) said substrate comprises single crystal silicon; and

b) said elongated channel comprises silicon epitaxially grown from said substrate.

11. A field effect transistor as defined in Claim 1 wherein said elongated channel is substantially orthogonal to said upper substrate surface.

12. A method for forming a field effect transistor comprising the steps of:

a) providing a conductive substrate; then

b) etching said substrate to form an upstanding pillar adjacent a substantially-planar upper surface of said etched substrate; then

c) forming a stack of substantially-planar layers of material adjacent said pillar, said stack of material comprising a first insulator layer adjacent said upper surface of said etched substrate, a gate layer of conductive material overlying said first insulator layer and a second insulator layer overlying said gate layer; then

d) etching said pillar to the level of said substantially-planar upper surface of said etched substrate to form a upstanding pore within said stack; then

e) forming a gate insulator layer at the interior of said upstanding pore; then

f) forming an upstanding channel of semiconductor material having a top region and a bottom region interior of said gate insulator layer; and then

g) heavily doping said top region of said upstanding channel of semiconductor material.

13. A method as defined in Claim 12 wherein the step of etching said substrate further includes the steps of:

a) masking said substrate with a nanoparticle; and then

b) directionally etching said masked substrate whereby whereby said pillar is a nanopillar and said pore is a nanopore.

14. A method as defined in Claim 13 further including the step of depositing a layer of conductive material in contact with said gate layer at the interior of said nanopore.

15. A method as defined in Claim 13 further characterized in that the step of forming an upstanding channel of semiconductor material further includes the step of epitaxially growing said channel from said substrate.

16. A method as defined in Claim 15 wherein said substrate comprises single crystal silicon.

17. A method as defined in Claim 13 wherein said substrate comprises a highly-doped semiconductor material.

18. A method as defined in Claim 17 wherein said substrate comprises highly-doped silicon.

19. A method as defined in Claim 12 wherein said gate layer comprises a metal.

20. A method as defined in Claim 12 wherein said gate layer comprises a highly-doped semiconductor.

21. A method for forming a field effect transistor comprising the steps of:

a) providing a substrate of semiconductor material; then

b) etching said substrate to form an upstanding pillar, adjacent a substantially-planar upper surface of said etched substrate; then

c) creating a conductively-doped region within said etched substrate substantially and immediately beneath said pillar; then

d) forming a stack of substantially-planar layers of material adjacent said pillar, said stack of materials comprising a first insulator layer adjacent said upper surface of said etched substrate, a gate layer of conductive material overlying said first insulator layer and a second insulator layer overlying said gate layer; then

e) etching said pillar to the level of said substantially-planar upper surface of said etched substrate to form an upstanding pore within said stack; then

f) forming a gate insulator layer interior to said upstanding pore; then

g) forming an upstanding channel of semiconductor material having a top region and a bottom region interior of said gate insulator layer; and then

h) heavily doping said top region of said upstanding channel.

22. A method as defined in Claim 21 wherein the step of etching said substrate further includes the steps of:

a) masking said substrate with a nanoparticle; and then

b) directionally etching said masked substrate whereby whereby said pillar is a nanopillar and said pore is a nanopore.

23. A method as defined in Claim 22 further including the step of depositing a layer of conductive material in contact with said gate layer at the interior of said nanopore.

24. A method as defined in Claim 22 further characterized in that the step of forming an upstanding channel of semiconductor material further includes the step of epitaxially growing said channel from said substrate.

25. A method as defined in Claim 24 wherein said substrate comprises single crystal silicon.

26. A method as defined in Claim 21 wherein said gate layer comprises a metal.

27. A method as defined in Claim 21 wherein said gate layer comprises a highly-doped semiconductor.

28. A method for forming a field effect transistor comprising the steps of:

a) providing a substrate having an upper surface; then

b) forming a stack of substantially-planar layers of material on said substrate, said stack comprising a first insulator layer adjacent said upper surface of said substrate, a gate layer of conductive material overlying said first insulator layer and a second insulator layer overlying said gate layer; then

c) forming an overlayer on top of said second insulator layer; then

d) masking said overlayer with a nanoparticle; then

e) directionally etching said overlayer to form an upstanding nanopillar on top of said second insulator layer; then

f) depositing a second overlayer on top of said second insulator layer and said upstanding nanopillar; then

g) removing said second overlayer to the top of said upstanding nanopillar; then

h) removing said nanopillar to leave an upper nanopore within said second overlayer defining an etch mask; then

i) directionally etching a lower nanopore to said upper surface of said substrate; then

j) removing said second overlayer; then

k) forming a gate insulator layer at the interior of said upstanding nanopore; then

l) forming an upstanding channel of semiconductor material having a top region and a bottom region interior of said gate insulator layer; and then

m) heavily doping said top region of said

upstanding channel of semiconductor material.

29. A method as defined in Claim 28 further including the step of depositing a layer of conductive material in contact with said gate layer at the interior of said nanopore.

30. A method as defined in Claim 28 further characterized in that the step of forming an upstanding channel of semiconductor material further includes the step of epitaxially growing said channel from said substrate.

31. A method as defined in Claim 30 wherein said substrate comprises single crystal silicon.

32. A method as defined in Claim 28 wherein said gate layer comprises a metal.

33. A method as defined in Claim 28 wherein said gate layer comprises a highly-doped semiconductor.